REMARKS

The Examiner rejected claims 1, 6, 8, 11, 12, 14, 15 and 19 under 35 U.S.C. §103(a) as being unpatentable over Hsu et al. (USP 6,844,750) in view of Stubbs et al. (USP 6,597,619).

The Examiner rejected claims 2, 3, 13 and 16 under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (USP 6,844,750) et al. in view of Stubbs et al. (USP 6,597,619) and Mancatis (USP 6,462,527).

The Examiner rejected claims 5, 10 and 18 under 35 U.S.C. 103(a) as being unpatentable Hsu et al. (USP 6,844,750) et al. in view of Stubbs et al. (Usp 6,597,619) and Maneatis (USP 6,462,527) and Shyr et al. (USP 6,472897).

The Examiner rejected claims 7, 9 and 20-22 under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (USP 6,844,750) et al. in view of Stubbs et al. (Usp 6,597,619) and Persun et al. (US 2004/0236200).

Applicants respectfully traverse the 35 U.S.C. §103(a) rejections with the following arguments.

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35 USC § 103

As to claims 1 and 15, the Examiner states that "Hsu et al.'s figure 12 shows a circuit comprising a current mirror (1206, 1208) coupled to a tunneling leakage monitor (1210), the tunneling leakage monitor including a tunneling leakage monitoring device (1210), the current mirror adapted to force a current through the tunneling leakage device to a predetermined current value, the current comprising only tunneling leakage current. Thus, figure 12 shows all limitations of the claim except for a voltage buffer coupled to the leakage monitor. However, Stubbs et al.'s figure 3 shows a buffer circuit for reducing output noise. Therefore, it would have been obvious to one having ordinary skill in the art to couple Stubbs et al.'s circuit figure 3 to the output of Hsu et al.'s figure 12 for the purpose of reducing output noise. Thus, the modified Hsu et al.'s further shows a voltage buffer (Stubbs et al.'s 200) coupled to the leakage monitor, the voltage buffer adapted to generate an output voltage based on a voltage level developed across the leakage monitoring device when the current is at the predetermined current value."

Applicants contend that claims 1 and 15, as amended, are not anticipated by Hsu et al. in view of Stubbs et al. because Hsu et al. in view of Stubbs et al. does not teach or suggest each and every feature of claims 1 and 15. For example, Hsu et al. in view of Stubbs et al. does not teach "said tunneling leakage monitor circuit comprising a first PFET, a second PFET, a first NFET and a second NFET, sources of said first and second PFETS connected to a voltage source, gates of said first and second PFETs and said drain of said first PFET connected to a drain of said first NFET, a drain of said second PFET connected to a gate of said second NFET, sources of said first and second NFETs and a drain of said second NFET connected to ground."

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First, Applicants point out that the combination of Hsu et al. in view of Stubb et al. does not teach or suggest the combination and interconnections of NFETs and PFETs as in Applicants claims 1 and 15."

Second, the circuit Hsu et al. FIG. 12 cannot measure tunneling leakage current because it is wired incorrectly to do so. The current flow in dielectric tunneling leakage current must be measured from the gate electrode to either or both of the source and drains. Sub-threshold leakage voltage the current must be measured between the source and drains. Further, because of the bias applied by 1202 to the gate of device 1210, any tunneling leakage current actually flowing through device 1210 would be undetectable because of the huge differences in current values between sub-threshold leakage currents and tunneling leakage currents. However, Applicants claims 1 and 15 clearly limits the type of current to "tunneling leakage current."

Based on the preceding arguments, Applicants respectfully maintain that claims 1 and 15 are not unpatentable over Hsu et al. in view of Stubbs et al. et al. and are in condition for allowance. Since claims 2, 3, 5, 6, 23 and 24 depend from claim 1 and claims 16, 17, 18, 25 and 26 depend from claim 15, Applicants respectfully maintain that claims 2, 3, 5, 6, 23 and 24 and claims 16, 17, 18, 25 and 26 are likewise in condition for allowance.

As to claim 8, the Examiner states "The modified Hsu et al.'s figure 12 shows a method comprising: forcing a current (output of Hsu et al.'s 1208) of known value only through a dielectric layer of a tunneling current leakage monitor device (1210) to provide a voltage signal (Vsense); and regulating (by using Stubbs et al.'s figure 3) on-chip power supply of the integrated circuit chip based on the voltage signal."

Applicants contend that claim 8, as amended, is not anticipated by Hsu et al. in view of Stubbs et al. because Hsu et al. in view of Stubbs et al. does not teach each and every feature of

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claim 8. For example Hsu et al. in view of Stubbs et al. does not teach "said tunneling leakage monitor circuit comprising a first PFET, a second PFET, a first NFET and a second NFET, sources of said first and second PFETS connected to a voltage source, gates of said first and second PFETs and said drain of said first PFET connected to a drain of said first NFET, a drain of said second PFET connected to a gate of said second NFET, sources of said first and second NFETs and a drain of said second NFET connected to ground."

Applicants maintain , that the arguments presented *supra* in regards to claims 1 and 15, are applicable to claim 8.

Based on the preceding arguments, Applicants respectfully maintain that claim 8 is not unpatentable over Hsu et al. in view of Stubbs et al. et al. and is in condition for allowance. Since claims 10-14 depend from claim 8, Applicants respectfully maintain that claims 10-14 and are likewise in condition for allowance.

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CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0457.

Respectfully submitted,
FOR: Abadeer et al.

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